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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/035,474 | 10/25/2001 | John E. Barth JR. | FIS920010094US1 | 5062 |

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INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

| EXAMINER | |
|---|---|
| TRIMMINGS, JOHN P | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2133 | |

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/035,474 | BARTH ET AL. | |
| | Examiner | Art Unit | |
| | John P. Trimmings | 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *2-5,8,9,11,12,14-17 and 20-27* is/are pending in the application.

4a) Of the above claim(s) *8,9 and 27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-5,11-12,14-17,20-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This office action is in response to the applicant's RCE and amendment dated 6/29/2005.

The applicant canceled claims 1, 6, 7, 10, 13, 18 and 19.

The applicant has added Claims 25, 26 and 27 as new claims.

Claims 2-5, 8-9, 11-12, 14-17 and 20-27 are pending in this office action.

### *Continued Examination Under 37 CFR 1.114*

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/29/2005 has been entered.

### *Election/Restrictions*

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 25, 26, 2-5, 11-12, 14-17 and 20-24 drawn to a memory repair method/apparatus, the method/apparatus limited to execution during normal memory operation, classified in class 714, subclass 718.

II. Claims 8, 9 and 27, drawn to a memory repair method, the method limited to execution only during non-normal memory operation, classified in class 714, subclass 718.

The inventions are distinct, each from the other because of the following reasons:

Inventions II and I are unrelated. Inventions are unrelated if it can be shown that they are not disclosed as capable of use together and they have different modes of operation, different functions, or different effects (MPEP § 806.04, MPEP § 808.01). In the instant case the different inventions are mutually exclusive, i.e.; they cannot exist together because of opposing limitations, specifically, of executing during normal versus executing during non-normal operation of the circuit.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

During a telephone conversation with Daryl K. Neff on 7/21/2005, a provisional election was made without traverse to prosecute the invention of Group II, claims 25, 26, 2-5, 11-12, 14-17 and 20-24. Affirmation of this election must be made by applicant in replying to this Office action. Claims 8, 9 and 27 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim

remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

### *Response to Arguments*

2. Applicant's arguments with respect to claims 25, 26, 2-5, 11-12, 14-17 and 20-24 have been considered but are moot in view of the new grounds of rejection (see below).

### *Claim Rejections - 35 USC § 103*

3. Claims 2-5, 14-16 and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto et al., U.S. Patent No. 5278839 (Matsumoto), in view Holman et al., U.S. Patent No. 6519735 (Holman), in view of Lee et al., U.S. Patent No. 5748543 (Lee), and further in view of Saito et al., U.S. Patent No. 6532181 (Saito).

As per Claims 25 and 26:

Matsumoto teaches a method for identifying a failed memory element within an integrated circuit memory and repairing the memory (column 1 lines 53-56), based on an integrated circuit comprising: automatically identifying and recording locations of failures (column 4 lines 67-68 and column 5 lines 1-29) within said integrated circuit memory. But Matsumoto fails to further teach error detection with ECC means. But Holman does teach this feature; by storing data bits and error correction code (ECC) check bits to individual locations of said memory thereafter retrieving data bits and ECC check bits from said individual locations (Abstract and FIG.1 and column 1 lines 56-67 and column 2 lines 1-7, where the location of a defective cell in a memory is

provided by an ECC means); recording at least single-bit failure locations in said integrated circuit memory based on ECC processing said retrieved data bits together with said retrieved ECC check bits (column 1 lines 56-67 and column 2 lines 1-7). And in column 1 lines 48-54, the advantage stated in Holman is a better method of locating a defective memory cell prior to isolating the failed bit. One with ordinary skill in the art, motivated as suggested, would have found it obvious to use the compact bit failure system of Holman to located failures in a self-repairing device such as in Matsumoto. But Matsumoto and Holman, in failing to further teach the applicant's claim, are supplemented by Lee wherein; based on said recorded failure locations, using first logic circuits within said integrated circuit to automatically identify a failed memory element in one bank of said plurality of banks (Abstract and column 3 lines 31-43), and while using at least second logic circuits within said integrated circuit to automatically replace said failed memory element in said one bank with a redundant element (spare substituting circuit in Abstract). It would have been obvious to additionally modify the circuit and method of Matsumoto and Holman by adding the failure replacement units taught by Lee into the circuit, because Lee in column 2 lines 27-33, also boasts the advantage of repair after device packaging. One with ordinary skill in the art at the time of the invention, motivated as suggested above for Lee et al., would combine the systems in order to have post manufacture testing and repair capabilities. But neither Matsumaoto, Lee nor Holman teach providing an integrated circuit memory having a plurality of banks and asserting a busy signal for said one bank while servicing memory access requests by banks of said plurality of banks other than said one bank (the other

bank, which may be under repair). But in the analogous art of Saito, these features are presented. A multiple-bank memory (example; FIG.3 BANK0, BANK1) is operated where the banks are provided with busy signals so that while one bank is busy (as in a repair cycle write to the bank) the other bank may be accessed (column 19 lines 59-67 and column 20 lines 1-22). And in the Summary of the Saito invention, an advantage stated was; "a memory cell array control circuit which controls the memory cell array so that while a data write operation or data erase operation is carried out in one of the banks, a data read operation can be carried out in the other banks". One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to improve the availability of a memory by including the bank accessibility along with a busy signal as taught by Saito in the invention of Matsumoto, Holman and Lee.

As per Claims 2 and 14:

Matsumoto further teaches the method of Claim 25 and 26 wherein said integrated circuit memory is of the type selected from dynamic random access memory (DRAM), static random access memory (SRAM), and electrically erasable programmable read only memory (EEPROM) including flash memory (column 1 lines 6-16). And in view of the motivation previously stated, the claims are rejected.

As per Claim 3 and 24:

The method of Claim 25 and 26 wherein said failed memory element is replaced with a redundancy element selected from the group consisting of at least row

redundancy element and column redundancy element is further taught by Lee et al. in the Abstract. And in view of the motivation previously stated, the claims are rejected.

As per Claim 4, 5, 15 and 16:

The method of Claim 25 and 26 wherein said electrically alterable circuit connections include at least one selected from the group consisting of electronic fuse and electronic anti-fuse is also taught by Lee et al. in the Abstract. And in view of the motivation previously stated, the claims are rejected.

4. Claims 11, 12, 17, 20, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto et al., U.S. Patent No. 5278839, in view of Lee et al., U.S. Patent No. 5748543, in view of Holman et al., U.S. Patent No. 6519735, and further in view of Sait et al., U.S. Patent No 6532181 as applied to Claims 25 and 26 above, and further in view of Eaton et al., U.S. Patent No. 4939694.

As per Claims 11 and 17:

References Matsumoto et al., Lee et al. and Holman et al. and Saito et al., fail to further teach the method and circuit of claims 25 and 26 wherein said memory failures are automatically recorded, said failure patterns automatically identified, and said failed memory element is automatically replaced while said integrated circuit is in a normal operational mode. In an analogous art however, Eaton et al. does teach this feature in column 7 lines 1-28. It would have been obvious to modify the circuit and method of Matsumoto et al. to include DRAM type memories and testing to occur under normal conditions thereby reducing cost. And in column 2 lines 14-17, Eaton et al. recites the

advantage of less costly testing expense as well as improved product yield. And one with ordinary skill in the art at the time of the invention, motivated by Eaton et al., would combine the references to reduce cost, and so the claims are rejected.

As per Claim 20:

Eaton et al. also teaches the method and circuit of claim 26 wherein said non-normal operational mode is of a type selected from power-up mode or power-down mode (column 7 lines 38-43). And in view of the motivation previously cited for Eaton et al., the claim is rejected.

As per Claim 22:

The method and circuit of claim 20 wherein said integrated circuit memory is of the DRAM type and wherein said locations are automatically recorded while said integrated circuit is in a normal operational mode is further taught by Eaton et al. in column 1 lines 15-16 and column 7 lines 1-28. It would have been obvious to modify the circuit and method of Matsumoto et al. to include DRAM type memories and testing to occur under normal conditions thereby reducing cost. And in column 2 lines 14-17, Eaton et al. recites the advantage of less costly testing expense as well as improved product yield. And one with ordinary skill in the art at the time of the invention, motivated by Eaton et al., would combine the references to reduce cost, and so the claim is rejected.

As per Claims 12 and 23:

The method and circuit of claims 11 and 26 wherein said failed memory element is automatically replaced when said integrated circuit remains installed within a product

for normal use is also taught by Eaton et al. in column 7 lines 43-55. And in view of the motivation above, the claims are rejected.

5. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto et al., U.S. Patent No. 5278839, in view of Lee et al., U.S. Patent No. 5748543, in view of Holman et al., U.S. Patent No. 6519735, and further in view of Saito et al., U.S. Patent No. 6532181 as applied to Claim 26, and further in view of Hughes et al., U.S. Patent No. 6691252. The circuit of claim 26 wherein said integrated circuit memory is incorporated within an integrated circuit having a microprocessor is taught by Hughes et al. in column 9 lines 59-65. It would have been obvious to modify the circuit of Matsumoto et al. to additionally provide failure recovery to embedded memories within a microprocessor. And Hughes et al., in column 3 lines 55-59 recites an advantage being the capability to repair a fault at the same time testing continues to be executed within the circuit. One with ordinary skill in the art at the time of the invention, motivated by Hughes et al. as suggested, would combine the references in order to simultaneously repair while operating the system, and so the claim is rejected.

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

jpt

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100